

國立交通大學試題紙

一百零七學年度第二學期
博士班資格考

科目：計算機架構 A

日期：108 年 7 月 30 日 第 1 頁 共 2 頁

請“✓”明 ✓不可看書 可看書

* 請將答案依題號順序寫入答案卷

答題時字跡需工整，否則不予計分。Write your answers legibly; otherwise you will get zero score.

1. (10%)
 - (a) (6%) Describe the characteristics, one main advantage and one main disadvantage for each of the following architectures: *stack*, *accumulator*, and *general-purpose-register* architectures.
 - (b) (4%) Describe the four properties of instruction set architecture design which may help compiler writer to design a compiler that will generate efficient and correct code.
2. (8%) Give the equation to calculate the CPI (clocks per instruction) for a pipelined processor,
$$\text{Pipeline CPI} = \text{Ideal pipeline CPI} + \text{Structural stalls} + \text{Data hazard stalls} + \text{Control stalls}$$

For each of the following techniques, which ones of the components of the CPI equation does the technique affect? If a technique affects data hazard stalls, please specify the dependence types (true, anti, and/or output dependences) of the hazards.

 - (a) Forwarding and bypassing
 - (b) Delayed branches
 - (c) Branch prediction
 - (d) Loop unrolling
3. (6%) Given a computer implemented in multiple-cycle implementation with a clock cycle time of 5 ns, assume that it uses 4 cycles for ALU operations, 2 cycles for branches, 4 cycles for memory store operations, and 5 cycles for memory load operations, and the relative frequencies of these operations are 40%, 30%, 10%, and 20%, respectively. Design the computer as a 5-stage pipelined implementation. After the stages are split by functionality, the measured times were IF, 4 ns; ID, 3 ns; EX, 3.5 ns; MEM, 5 ns; and WB, 2 ns. The pipeline register delay is 0.4 ns.
 - (a) What is the average instruction execution time for the multiple-cycle machine?
 - (b) What is the clock cycle time of the 5-stage pipelined machine? If there was no hazard in this pipeline, what is the speedup of the pipelined machine over the multiple-cycle machine?
 - (c) If there will be a stall due to data hazard every 5 instructions and a stall due to the control hazard of each branch instruction in this 5-stage pipelined machine, what are the CPI and the average instruction execution time for the pipelined machine, and what is the speedup of the pipelined machine over the multiple-cycle machine?

◎請用深黑色鋼筆或原子筆出題

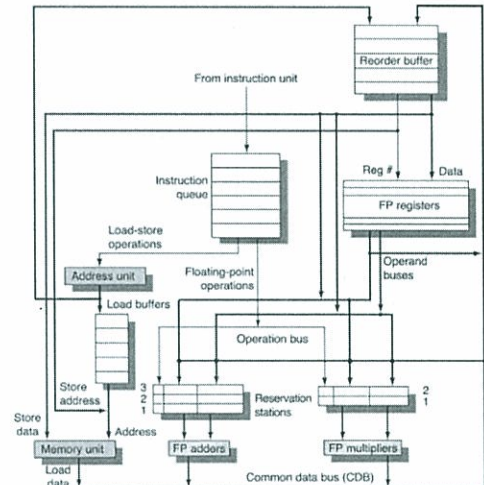
命題老師簽名：

科目：計算機架構 A

日期：108 年 7 月 30 日 第 2 頁 共 2 頁

4. (8%) Given the structures of the **Tomasulo algorithm with reorder buffer (ROB)**,

- (4%) Describe the key idea of this algorithm and the main purposes of using reservation stations (RS) and ROB in this structure,
- (4%) Describe the following four steps involved in instruction execution of this algorithm: *Issue*, *Execute*, *Write result*, *Commit*.



- (6%) Describe the characteristics, one main advantage, and one main disadvantage for each of the following multiple-issue approaches: *speculative superscalar* and *VLIW* (Very Long Instruction Word).
- (12%)
 - (6%) Describe the characteristics of the following two classes of MIMD multiprocessors and draw the block diagram of the basic structure for each of them: *centralized shared-memory multiprocessor* and *distributed shared-memory multiprocessor*.
 - (6%) Describe and compare the following two cache coherence protocols: *snooping* and *directory-based*.

科目：計算機架構 B

日期：108 年 7 月 30 日 第 1 頁 共 1 頁

請 "✓" 明 ✓不可看書 可看書

* 請將答案依題號順序寫入答案卷

答題時字跡需工整，否則不予計分。Write your answers legibly; otherwise you will get zero score.

1. (10%)
In designing the ISA (Instruction Set Architecture) for a general-purpose CPU, seven ISA decisions need to be made. List **any five** of these decisions, and give each some explanation.
2. (10%)
Three primary computer system concerns related to power and/or energy are: 1. *Maximum required power*, 2. *Sustained power consumption*, and 3. *Energy and its efficiency*. For each of these concerns, **what** system design aspect (or component) will be affected, and **why**?
3. (10%)
(a) List and define the three cache miss types for a uniprocessor computer system.
(b) We run a program on a uniprocessor computer system with a particular cache, and get a list of cache misses. Explain how we can identify each of the cache miss as belonging to what miss type. Make your answer clear and easy to understand.
4. (10%)
(a) List the **four "memory hierarchy" questions**, together with **possible options for dealing with each one** of the questions. (Note: the memory hierarchy can be any, not limited to cache memory.)
(b) For **main memory** design in a **virtual memory system**, for each of the four questions, usually **what** option(s) do we choose to use? And **why** do we do so? (Give enough support.)
5. (10%)
A program spends 10% of its execution time on initialization and wrapping up which are both strictly sequential, 20% on data transfer (Loads and Stores, assuming no CPU time overhead here), and the rest 70% on computation (data processing).
(a) If we **ONLY** refine the computation algorithms to make the computation part 20 times faster, what will the speedup be?
(b) If we do not refine the computation algorithms but **ONLY** replace the CPU with another one which is two times faster, what will the speedup be?
(c) Without improving the memory system, what will the speedup upper bound be?